UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,138	03/01/2002	Stephen Liscinksy	43269	2695

7590 05/05/2004

Roylance, Abrams, Berdo & Goodman, L.L.P.
Suite 600
1300 19th Street, N.W.
Washington, DC 20036

EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20040415

Application Number: 10/085,138
Filing Date: March 01, 2002
Appellant(s): LISCINKSY, STEPHEN

Peter L. Kendall
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 5,2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that Group I (claims 1 – 16) and Group II claims (17 – 18) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

US 3,535,591	Holmquest	10-1970
US 5,224,010	Tran et al.	06-1993
US 5,642,052	Earle	06-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

a). Claims 1, 4 - 6, 11, 12, 14 - 18 are rejected under 35 U.S.C. 103(a) being unpatentable over Holmquest in a view of Tran et al. (US 5,224,0100).

Regarding Claim 1, Holmquest discloses most of the elements of the claim including a first, second and third sensing circuits (elements 12, 13 and 14 in Fig. 2a) for detecting a voltage levels for particular phases of the AC power signal and comparing the voltage levels of the phases to a threshold value (col. 2, lines 68 – 72); it further discloses a delay circuit delaying a result of operation of the sensing circuits for a predetermined time (element 22 in Fig. 2b, col. 4, lines 7 – 13) and an activation circuit indicative of whether the predetermined period of time has elapsed and the voltage levels have met the threshold value (element 107 in Fig. 2b, col. 4, lines 13 – 22). However, even though his delay circuit can act at the time of power-up, it is not explicitly disclosed. Tran et al. discloses a power supply supervisor with independent power-up delays (shown in Fig. 2 and 3a, col. 6, line 63 through col. 8, line 7), which delays enabling shutdown operations until establishment of adequate voltages on the power supply bus thus allowing for a power supply to stabilize and ignoring faults for a brief period of time. His power-up delay is independent and does not delay normal shutdown operations of the system. Both patents have the same problem solving area, namely providing three-phase power supervision and protection. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Holmquest solution by introducing the independent delay circuit of Tran et al., because as Tran et al. states (col. 1, lines 20 – 32), to avoid false shut downs, the fault conditions should be reliably distinguished from the power-up state.

As per Claim 12, the claimed method is inherent in the structure disclosed in Claim 1 and rejected accordingly.

Regarding Claim 4, Holmquest discloses the supervisory system, wherein the indication signal represents a first negative indication that the input AC does not meet the threshold value.

Regarding Claims 5 and 14, Tran et al. discloses the supervisory system, wherein the predetermined period of time provides for stabilization of capacitors (elements Csd and Coc in Fig. 2) in the circuit upon initially powering the circuit. The delay element capacitor (element Cpg in Fig. 3a) asserts its normal stable value after initial transient process associated with powering up the circuit. Both patents have the same problem solving area, namely providing three-phase power supervision and protection. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Holmquest solution by introducing the independent delay circuit of Tran et al., because as Tran et al. states (col. 1, lines 20 – 32), to avoid false shut downs, the fault conditions should be reliably distinguished from the power-up state.

Regarding Claim 6, Holmquest discloses the supervisory system, wherein in response to receiving the first and second positive indications, i.e. the input AC signal meets the threshold value and the predetermined time period elapsed the activation circuit outputs the AC power signal. When no error signal occurs on the error bus (element 21 in Fig. 2a and 2b) the transistors (elements 106 and 107 in Fig. 2b) remain

in saturation, the activation element (element 23 in Fig. 2b) remains reenergized and AC signal remains being supplied as before.

Regarding Claims 7 and 16, Holmquest discloses the supervisory system, wherein each of the sensing circuits has to detect a proper voltage level in a respective phase before a positive indication is provided to the activation circuit. According to him, a positive indication (lack of signal on bus 21 in Fig. 2a and 2b) is provided only when none of three sensing circuits (elements 12 – 14 in Fig. 2a) sends an error signal to the bus (col. 4, lines 7 – 22).

Regarding Claim 11, Holmquest discloses the supervisory system reacting to the fault condition, such as a low phase voltage level (elements 12 – 14 in Fig. 2a, col. 2, lines 68 – 72).

Regarding Claim 17, Holmquest discloses a monitoring system capable of detecting open circuit in any of the three phases (phases A, B, and C in Fig. 1). Eventually it will give the failure indication, when more that one phase is open, as well. It is because the open circuit condition is an extreme case of undervoltage conditions, which are detectable by the circuit.

As per Claim 18, the claimed method is inherent in the structure disclosed in Claim 17 rejected accordingly.

b) Claims 8 - 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmquest in a view of Tran et al. and further in a view of Earle (US 5,642,052). As was stated above, Holmquest and Tran et al. disclose all the elements of Claim 1. They

further disclose an element of Claim 8, namely a contactor coil connected to the activation circuit (element 25 in Fig. 1 and 23 in Fig. 2b). However they do not disclose a plurality of ground fault interrupter receptacles.

Earle discloses the ground fault interrupter receptacles (see Fig. 1 and col. 1, lines 65 – 67, col. 4, lines 1 - 2). It further discloses a voltage measurement circuit for a GFCI (element 106 in Fig. 5b, col. 8, lines 27 – 50). Both patents have the same problem solving area, namely providing efficient protection for AC fed equipment. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used combination of the GFCI circuits together with the Holmquest polyphase electric supply protection system, because as Earle states (col. 2, lines 3 – 21), use of GFCI necessitates a voltage testing to ensure a proper values of the voltage in an AC receptacle.

Regarding Claim 9, in the Holmquest polyphase electric supply protection system combined with the GFCI the GFCI receptacles are being protected via Holmquest supply protection system.

Regarding Claim 10, Earle disclose use of its circuit as a tester for allowing testing of AC power signals (col. 2, lines 14 – 21).

c) Claims 2, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmquest in a view of Tran et al. and further in a view of Court Decision *In re Aller,* 105 USPQ 233.

As was stated above, Holmquest and Tran et al. disclose all the elements of Claims 1 and 12. However, regarding Claims 2 and 13, they do not disclose a predetermined time period between one and two seconds. As was stated above, Holmquest discloses a time delay, but does not specify a particular value. The Court Decision states that discovering the optimum or workable ranges involves only routine skill in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have selected time delay of one to two seconds, because as the cited Court Decision states, where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

d) Claims 3, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmquest in a view of Tran et al. and further in a view of Court Decision *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

As was stated above, Holmquest and Tran et al. disclose all the elements of Claims 1 and 12. However, regarding Claims 3 and 15, they doe not disclose a threshold value of 12 volts. As well known in the art, most of designers to measure/compare the AC line voltage use to scale it down to low voltage value, because processing of low voltage values is easier and cheaper. Accordingly, Holmquest scales the phase voltages down and compares them to the zener diodes threshold (elements 42 – 44 in Fig. 2a, col. 2, lines 67 – 73). As to selection of particular value of 12 volts, the Court Decision states that discovering an optimum value of a

result effective variable involves only routine skill in the art. An optimum value in this case is a degree of scaling down the phase voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have selected an optimum value of scaling don the phase voltage and set the 12 volts threshold, because as the cited Court Decision states, that discovering an optimum value of a result effective variable involves only routine in the art.

(11) R sponse to Arguments

According to Applicant's request Claims of the first group of Claims (Claims 1 – 16) should stand or fall together, the same was requested for the second group of Claims (Claims 17, 18). Therefore Claim 1 is representative of Group I (Claims 1 – 16). As to Group II (Claims 17, 18), Claim 17 is representative of the Group.

1. Applicant misrepresents the Examiner position (page 4, lines 20 – page 5, line 2) saying: "The Examiner admits that the Holmquest does not clearly state when the delay occurs. However, the Examiner relies on the combination of the Holmquest patent with the Tran patent to show that, in view of the cited art, it would have been obvious to delay the operation of the sensing circuits each time the supervisory circuit is powered on".

The Examiner position is that Holmquest discloses a delay at every triggering event including the power up process. Examiner does not see any reason in the Applicant's argument that would preclude using combination of two references.

2. Applicant alleges that none of the prior art discloses delaying initial operation of sensing circuits (page 4, lines 15 – 16).

Examiner response: Holmquest discloses delaying initial operation of sensing circuits; sensing circuits (elements 12 – 14 in Fig. 1) output signal is delayed by the delay circuit (element 22 in Fig. 1 and 2). Tran patent discloses delaying initial operation

of sensing circuits; sensing circuits (elements 24 and 26 in Fig. 2) output signal is delayed by the delay circuits (elements 34 and 38 in Fig. 2).

3. As per Applicant's argument that none of the references teach sensing circuits being able to detect fault conditions being selected from a group consisting of an open first second or third phase, e t c. (page 4, lines 16 – 19), Holmquuest discloses a voltage sensors for each phase. Opening of any phase will result in undervoltage condition in the phase, which is detectable by Holmquest circuits (undervoltage sensors, elements 12 – 14, one per phase, in Fig. 1).

4. Applicant's statement that the supervisory circuit in the Tran patent also includes sensing circuits (page 5, line 8) is correct but immaterial.

5. As to Applicant allegation that the Tran patent does not disclose delaying its own sensing circuits (page 5, line 10), it is wrong. The delay circuits of Tran are delaying the sensing circuits in a same way as Appellant's circuit, i.e. by delaying their output signals. In Applicant's invention, the sensing circuits include voltage protecting varistors (MOV11 – MOV13 in Fig. 1), rectifier bridges (elements DB21 – DB23), and comparators COMP11 – COMP 23); all these elements are positioned upstream from the delay circuit (element 106), which comes into play only after the sensors signals have underwent an analog to digital form conversion by COMP11 – COMP23 circuits in Fig. 1. The delay circuit delays a digital signal by control of the logic AND circuit (elements D31 – D33, D4 and R18 in Fig. 1). This is in exact accordance with the Tran patent, in which the sensing circuits (elements 24 and 26 in Fig. 2) generate the output

signal, which is delayed by the delay circuits (elements 34 and 38 in Fig. 2 of Tran et al.).

Part A.

6. Applicant argues (page 5, line 23 – page 6, line 2) that Holmquest patent discloses a delay, which "can be considered as a post-detection delay", rather than "a delay occurring prior to the sensing circuits being operational"(emphasis added).

Examiner points out that (I) the Applicant's sensing circuits (elements 104 in Fig. 1) are operational from the moment the power is applied. Therefore, the delay in his circuit does not occur prior to the sensing circuits being operational. (II) The Applicant's delay occurs in the AND circuit (elements R18, D31 – D33, D4 in Fig. 1) controlled by the delay circuit (element 106 in Fig.1); both positioned downstream from the sensing circuits (elements 104 in Fig.1). Therefore the Applicant's delay is the post-detection delay, as well. In view of (I) and (II), the Applicant's argument is wrong.

7. As to Applicant's argument that in Holmquest patent the delay time is variable page 6, lines 5 – 12), rather than fixed to a predetermined time (page 6, lines 13 – 16), the predetermined time delay is disclosed by Tran reference, which is proposed modification of primary reference, as we suggested. The predetermined delay times are set by values of capacitors (elements Cpg in Fig. 3a and Csd in Fig. 3b in Tran).

8. Regarding Applicant's argument that the delay in Tran patent is for DC power supply and not for sensing circuits (page 7, lines 4 – 9), Examiner's position is that purpose of the delay is not recited in the Claim 1, therefore the argument is moot. In the

event it is not moot, Tran discloses a predetermined period time delay, which is a power-up delay (see the patent title), serving exactly the same goal as the Applicant's invention, i.e. "delaying initial operation of sensing circuits", which meets Claim 1 language.

Part B

9. Applicant argues that none of the references teach sensing circuits being able to detect fault conditions being selected from a group consisting of an open first, second or third phase, e t.c. (page 8, lines 1 – 7).

Examiner response: Holmquuest discloses a voltage sensors for each phase. Opening of any phase will result in undervoltage condition in the phase detectable by Holmquest circuit (undervoltage sensors, elements 12 – 14, one per phase, in Fig. 1).

10. Applicant argues that: "the Earle patent does not disclose, teach or suggest a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on" Page 8, line 23 – page 9, line3).

Examiner response: Earle patent has not been used for rejection of either Claim 1 or 17, therefore the argument is moot.

However, in the event it is not moot, Examiner has never suggested that the Earle reference teaches the power-up delay. The reference was used since it discloses a ground fault interrupt circuit. As to Appellant's suggestion that the Earle reference should be disqualified because it does not teach all the limitations of the claim, the Court Decision *In re Keller*, 208 USPQ 871 (CCPA 1981), states that it has been held

that one cannot show non-obviousness by attacking references individually where the rejections are based on combinations of references.

Part C.

11. Examiner agrees with the following Appellant statement: "It is well established that there must be some motivation or incentive in the cited art to combine the teachings to arrive at the claimed invention as suggested in the Action" page 10, lines 8 – 9).

Accordingly, Examiner provided motivational statements, whenever it was needed to combine the references. The Appellant allegation that "The only suggestion of the claimed combination is in Appellant's disclosure" is wrong. Here are the motivational statement used in the Office Action:

Holmquest in view of Tran et al.:

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Holmquest solution by introducing the independent delay circuit of Tran et al., because as Tran et al. states (col. 1, lines 20 – 32), to avoid false shut downs, the fault conditions should be reliably distinguished from the power-up state.

Holmquest in view of Tran et al. and further in view of Earle:

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used combination of the GFCI circuits together with the Holmquest polyphase electric supply protection system, because as Earle states (col. 2, lines 3 –

21), use of GFCI necessitates a voltage testing to ensure a proper values of the voltage in an AC receptacle.

Appellant further attempts to disqualify the references collectively and individually.

12. Applicant: "None of the cited art discloses a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on" (page 10, lines 11 – 12).

Examiner Response: Appellant is wrong. It was shown above (paragraph 5), the Tran et al. reference discloses a delay circuit for delaying initial operation of sensing circuits for a predetermined period each time the supervisory circuit is powered on.

13. Applicant: "One of skill in the art would not be motivated to combine the Holmquest patent with the Tran patent or the Earle patent. While the Holmquest patent discloses a single phase testing system (emphasis added), the Earle patent also discloses a single phase testing system and the Tran patent discloses a DC power system. Thus, none of the prior art can distinguish between phases" (page 9,lines 17 – 20).

Examiner Response: This allegation is wrong. The Holmquest reference deals with polyphase system, the Patent title speaks for itself ("Monitoring system for polyphase electric supply system") and additionally there are three undervoltage sensors (elements 12 – 14 in Fig. 1, col. 2, lines 22 - 27), one per phase. As to the argument, that the Tran et al. reference deals with the DC power system, rather than

AC, the delay in both references, as well as in the Application, is exercised in the stage located downstream from the sensing circuits; the signal at this location has been subjected to rectification by the diodes/bridges and A/D conversion by the comparators. The delay circuits in both Tran et al. reference and in the Application deal with logic representation of the original signal. Therefore, at this point, an original shape of the voltage (AC or DC) is immaterial.

14. Applicant argues: "In addition, none of the prior art discloses delaying sensing circuits" (page 9, lines 20 – 21).

Examiner Response: This issue was addressed above (see discussion of Tran et al. reference, paragraph 5); Examiner showed that Tran et al. reference discloses delaying sensing circuits in the same way as disclosed by Applicant.

15. As to consistently repeated criticism that the references taken individually do not disclose all the claims limitations, this issue is addressed by the Court Decision *In re Keller*, 208 USPQ 871 (CCPA 1981) with the following statement: it has been held that one cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Brian Sircus
SPE
Art Unit 2836

Zeev Kitov
April 29, 2004

Conferees:
Brian Sircus
Olik Chaudhuri OC

Roylance, Abrams, Berdo & Goodman, L.L.P.
Suite 600
1300 19th Street, N.W.
Washington, DC 20036